WHAT IS CLAIMED IS:

1. A magnetic memory device, comprising:

a memory cell array block having a plurality of magnetic memory cells arranged at intersections of wordlines, digit lines, and bitlines;

a reference memory cell array block having a plurality of magnetic memory cells arranged at intersections of reference wordlines, the digit lines, and a reference bitline, wherein one wordline is arranged at respective two adjacent wordlines;

a first bitline clamp circuit for making a predetermined first current flow to a selected magnetic memory cell in the memory cell array block through a bitline to which the selected magnetic memory cell in the memory cell array block is connected, according to data of the selected magnetic memory cell in the memory cell array block, the first bitline clamp circuit being coupled to the bitline;

second and third bitline clamp circuits for making a predetermined second current flow to selected magnetic memory cells in the reference memory cell array block through the reference bitline, the second and third bitline clamp circuits being coupled to an upper end and a lower end of the reference bitline, respectively; and

a sense amplifier for sensing and amplifying a third current on a first data line connected to the bitline and a fourth current on a

second data line connected to the reference bitline to judge the data of the selected magnetic memory cell in the memory cell array block.

2. The magnetic memory device as claimed in claim 1, wherein the first bitline clamp circuit is identical to the second and third bitline clamp circuits.

3. The magnetic memory device as claimed in claim 2, wherein the first bitline clamp circuit compares a level of a voltage of the bit line with a level of a bitline clamp circuits to make the voltage of the bit line rise up to the level of the bitline clamp voltage; and wherein each of the second and third bitline clamp circuits compares a level of a voltage of the reference bitline with the level of the bitline clamp voltage to make the level of the voltage of the reference bitline rise up to the level of the bitline clamp voltage.

4. The magnetic memory device as claimed in claim 1, wherein the reference memory cell array block has high level "H" data and low level "L" data, which are stored in two magnetic memory cells coupled to the reference wordline, respectively.

5. The magnetic memory device as claimed in claim 1, further comprising first, second, and third current supply units for supplying respective constant currents to the reference bitline, the data line, and the reference data line, respectively.

6. A magnetic memory device, comprising:

a memory cell array block having a plurality of magnetic memory cells arranged at intersections of wordlines, digit lines, and bitlines;

a reference memory cell array block having a plurality of magnetic memory cells arranged at intersections of reference wordlines, the digit lines, and a reference bitline, wherein two magnetic memory cells are arranged at either side of the reference bitline;

a first bitline clamp circuit for making predetermined first current flow to a selected magnetic memory cell in the memory cell array block through a bitline to which the selected magnetic memory cell in the memory cell array block is connected, according to data of the selected magnetic memory cell in the memory cell array block, the first bitline clamp circuit being coupled to the bitline;

second and third bitline clamp circuits for making a predetermined second current flow to selected magnetic memory cells in the reference memory cell array block through the reference

bitline, the second and third bitline clamp circuits being coupled to an upper end and a lower end of the reference bitline, respectively; and

a sense amplifier for sensing and amplifying a third current on a first data line connected to the bitline and a fourth current on a second data line connected to the reference bitline to judge the data of the selected magnetic memory cell in the memory cell array block.

7. The magnetic memory device as claimed in claim 6, wherein the first bitline clamp circuit is identical to the second and third bitline clamp circuits.

8. The magnetic memory device as claimed in claim 7, wherein the first bitline clamp circuit compares a level of a voltage of the bit line with a level of a bitline clamp circuits to make the voltage of the bit line rise up to the level of the bitline clamp voltage; and wherein each of the second and third bitline clamp circuits compares a level of a voltage of the reference bitline with the level of the bitline clamp voltage to make the level of the voltage of the reference bitline rise up to the level of the bitline clamp voltage.

9. The magnetic memory device as claimed in claim 6, wherein the reference memory cell array block has high level "H" data and low level "L" data, which are stored in two magnetic memory cells coupled to the reference wordline, respectively.

10. The magnetic memory device as claimed in claim 6, further comprising first, second, and third current supply units for supplying respective constant currents to the reference bitline, the data line, and the reference data line, respectively.